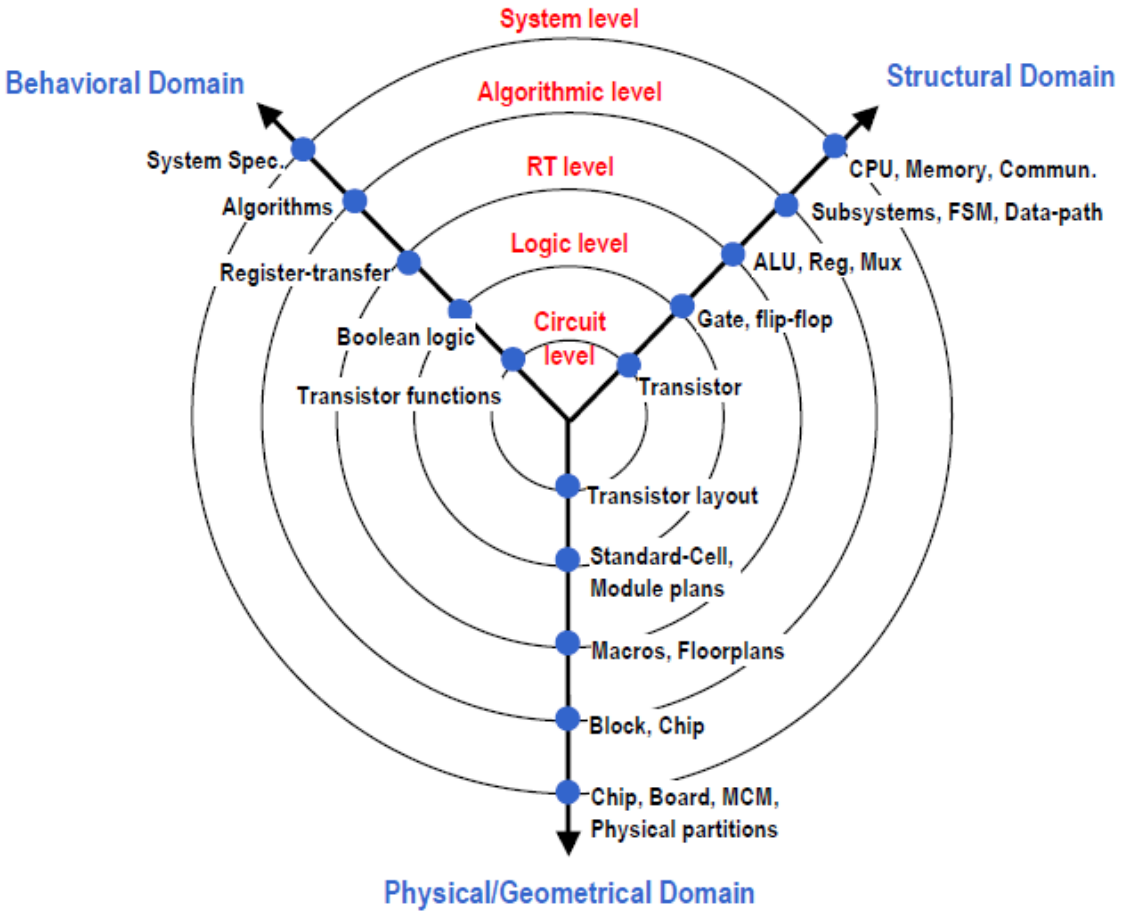
## Gajski-Kuhn Chart or Y-Chart




The **Gajski-Kuhn chart** (or Y diagram) describes the different perspectives in the hardware design. It depicts the different stages in development of an integrated circuit. According to this model, the development of hardware is perceived within three domains and five hierarchy levels. The 3 domains are shown by the three axes producing the Y. The 5 hierarchy levels are shown by the 5 circles. The outer circles are generalizations, the inner ones refinements of the same subject.

In the Y-chart, the three domains are:

1. **Behavioral:** This domain describes the temporal and functional behavior of a system.

2. **Structural:** A system is assembled from subsystems. Here the different subsystems and their interconnection to each other are listed for each level of abstraction.

3. **Geometrical/Physical:** In this domain, the geometric properties of the system and its subsystems are considered. So there are information about the size, the shape and the physical placement.

The five concentric circles characterize the hierarchical levels within the design process, with increasing abstraction from the inner to the outer circle. Aspects of the 5 levels in a Y-Chart are as mentioned below:

1. **System Level:** On the system level, basic properties of an electronic system are determined. For the behavioural description, block diagrams are used by making abstractions of signals and their time response. Blocks used in the structure domain are CPUs, memory chip, etc.

2. **Algorithmic Level:** The algorithmic level is defined by the definition of concurrent algorithms (signals, loops, variables, assignments). In the structural domain, blocks like ALUs are in use.

3. **Register-Transfer Level**: The register-transfer level (RTL) is a more detailed abstraction level on which the behaviour between communicating registers and logic units is described. Here, data structures and data flows are defined. In the geometric view, the design step of the floor plan is located.

4. **Logic Level:** The logic level is described in the behaviour perspective by Boolean equations. In the structural view, this is displayed with gates and flip-flops. In the geometric domain, the logical level is described bystandard cells.

5. **Circuit Level:** The behaviour of the circuit level is described by mathematics using differential equations or logical equations. This corresponds to transistors and capacitors up to crystal lattices.

The issue in hardware development is most often a top-down design problem. This is perceived by the three domains of behaviour, structure, and the layout that goes top-down to more detailed abstraction levels. The designer can select one of the perspectives and then switch from one view to another. The design process may not follow a specific sequence in Y – Chart/diagram.