Application Specific Integrated Circuit (ASIC)

Application Specific Integrated Circuits or ASICs are non-standard integrated circuits that are designed for a specific use or application. Here a complete system or product is integrated onto a chip and virtually no other components are required. The cost of designing an ASIC is very high and therefore they tend to be reserved for high volume products. But ASICs can be very cost effective for many applications where they are produced in large scale.

Types of ASICs:

1. Full-Custom ASICs
   In this type, the complete IC design and developments are customized by the designer. Full-custom offers the highest performance and lowest part cost. The advantages of full-custom design are reduced area (and therefore recurring component cost), better performance, increased reliability. The disadvantages of this type of ASIC are increased design time, complexity, increased non-recurring engineering costs, design expense, requirement of much higher skilled design team and highest risk. Examples of full-custom ASICs are mobile processor, sensor ICs, actuator ICs etc.

2. Standard-Cell–Based ASICs
   ASIC manufacturer creates functional blocks with known electrical characteristics, such as propagation delay, capacitance and inductance. Utilizing these functional blocks, standard cell of very high gate density and good electrical performance is designed. This gives a high degree of flexibility, provided that standard functions are able to meet the requirements. The significant advantage in Standard-Cell–Based ASICs is that this uses the manufacturer's cell libraries that have been used in potentially hundreds of other design implementations. Thus, there is very low risk associated than full custom design. Standard cells produce a design density that is cost effective, manufacturing time is also less (about eight weeks) and they can also integrate IP cores and SRAM effectively.

3. Gate-Array–Based ASICs
   This type of ASIC is the least customizable. This type of ASIC is ideal where a large number of standard functions are required which can be connected in a particular manner to meet the given requirement. Manufacturing lead time of Gate array based ASICs is between two days and two weeks.

Design Flow

A design flow is a sequence of steps to design an ASIC. Following are the steps of ASIC design:

1. Design entry: Using a hardware description language (HDL) or schematic entry, design is entered into an ASIC design system.
2. **Logic synthesis**: Using HDL (VHDL or Verilog) and a logic synthesis tool a netlist is produced. Netlist is a description of the logic cells and their connections.

3. **System partitioning**: In this step, a large system is divided into ASIC-sized pieces.

4. **Pre-layout simulation**: Functioning of the design is checked if it is working correctly.

5. **Floor planning**: The blocks of the netlist are arranged on the chip such a way that they take optimum space. In floor planning, distribution of connections and inter-effects of electrical parameters are also considered.

6. **Placement**: The locations of the cells in a block are decided.

7. **Routing**: The connections between cells and blocks are made.

8. **Extraction**: The resistance and capacitance of the inter-connects are determined.

9. **Post-layout simulation**: After the interconnections have been made, working of the design is tested.

---

**Advantages and Drawbacks of ASICs**

Following are advantages of an ASIC:

1. **Small in size**
   An ASIC is designed with proper floor planning. So, the size of an ASIC designed for a specific application is always smaller as compared to other programmable devices. Small size consequently leads to advantages in speed and power consumption.

2. **No routing Issues**
   There is no issue of routing for the end user in ASIC once it is designed.

3. **No timing Issues**
   Digital logic switching, analog effects and communication between blocks in the chip is faster in ASIC. Any configurable hardware must meet the timing requirement for the efficient operation of the circuit. Longer wires between components may affect the timing. Sometimes, over timing or under timing the new added design may yield erroneous result. An ASIC doesn’t have this problem.

4. **Less Power Consumption**
   ASIC consumes less power because logic operations are done within a chip; since smaller components have much smaller parasitic resistance, capacitance and inductance.
5. **Consistence and Reliable**  
An ASIC is consistent and reliable in its performance since it is designed by skilled designers to work for a specific task. Also, the probability for failure and impact of external environment are much less in integrated circuits. The lifetime of ASICs is much longer as they are IC based.

6. **Fully developed and functional**  
ASIC is designed from scratch to the fully functional stage. After its manufacturing no other configuration is required to be done.

**Drawbacks:**

Drawbacks of ASIC are:

1. **Not flexible**  
ASIC are made for a specific purpose. So, they are not flexible. But using PLDs, it is possible to achieve greater functionality with a simpler hardware design.

2. **Higher System Cost**  
By eliminating the ASIC design, system cost on a low-volume product can be lowered. Only for higher-volume products, the production cost of ASIC is lower. Reconfigurable computing systems are upgradeable and extend the useful life of the system. This reduces lifetime costs.

3. **Increased Time to Market**  
Increased time-to-market is the final drawback of ASIC. It is because designing of an ASIC is very complex and time consuming. Moreover before marketing, ASIC must be tested thoroughly and if fault is detected the IC has to be redesigned.

**ASIC versus FPGA**

<table>
<thead>
<tr>
<th>ASIC</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>An ASIC is a unique type of integrated circuit meant for a specific application.</td>
<td>An FPGA is a reprogrammable integrated circuit.</td>
</tr>
<tr>
<td>An ASIC can no longer be altered once created</td>
<td>FPGA is alterable</td>
</tr>
<tr>
<td>An ASIC wastes very little material, recurring costs are low.</td>
<td>FPGA is not efficient in terms of use of materials. A certain number of components are always wasted.</td>
</tr>
<tr>
<td>Cost of ASIC is low only when it is produced in large quantity.</td>
<td>FPGA is better than an ASIC when building low volume production circuits.</td>
</tr>
<tr>
<td>ASICs can't be used to test FPGAs.</td>
<td>ASICs are tested on FPGA before implementing.</td>
</tr>
<tr>
<td>ASICs are not suitable for research and development purposes, as they are not reconfigurable.</td>
<td>FPGAs are useful for research and development activities. Prototype fabrication using FPGA is affordable and fast.</td>
</tr>
</tbody>
</table>