SUCCESSIVE APPROXIMATION ANALOG TO DIGITAL CONVERTER

A successive approximation A/D converter consists of a comparator, a successive approximation register (SAR), a D/A converter and an output latch. The circuit diagram of a 4bit successive approximation A/D converter is shown in the figure below.

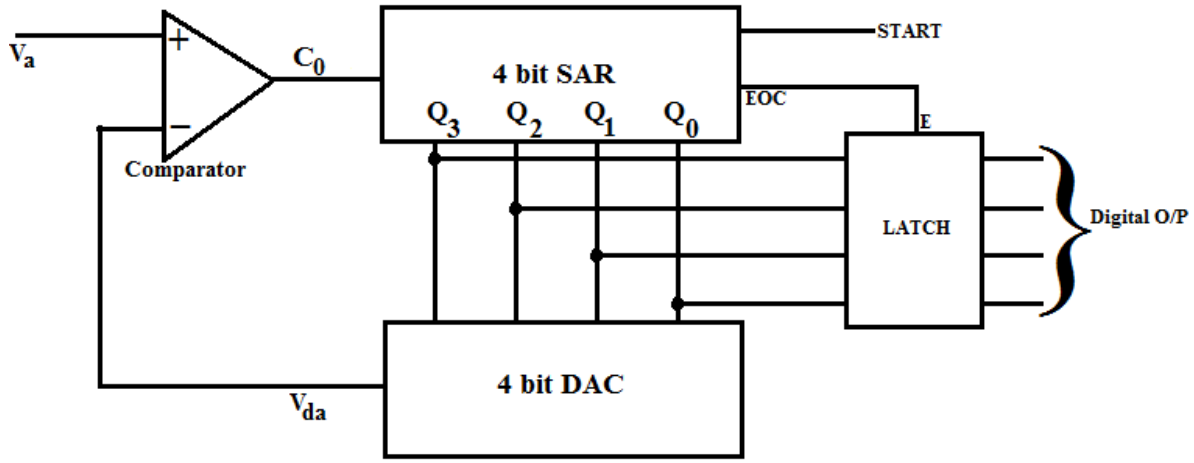

Figure: 4 bit successive approximation ADC

Working

At the start of a conversion cycle, the successive approximation register (SAR) is reset by making the START signal HIGH. The Most Significant Bit (MSB) of the SAR (Q_3) is set to HIGH, while other bits (Q_2, Q_1 and Q_0) are kept LOW. The output of the SAR is connected with the inputs of a Digital to Analog Converter (DAC). This DAC produces an analog equivalent of the applied input bits. Output of the DAC (V_{da}) is compared with the analog input (V_a) in the comparator. The comparator produces a LOW output (C_0=0) when output of the DAC (V_{da}) is greater than V_a. Then the MSB is cleared in the SAR and next highest bit (Q_2) is made HIGH. On the other hand, if V_a>V_{da}, C_0 is HIGH. In this condition, the MSB is left HIGH and the next highest bit (i.e. Q_2) is set to HIGH by the SAR. Thus, depending on the value of comparator output (C_0), the SAR will either keep or reset the next bit. This process continues until all the bits

are tried. After the last bit Q_0 is tried, the SAR produces an End of Conversion (EOC) signal to indicate the completion of the conversion process. This EOC signal is also connected with the enable input of the latch. So, when the process of analog to digital conversion gets over, EOC signal enables the latch and the digital data appear at the output of the latch.

Advantages of Successive Approximation ADC

i. Speed is high compared to counter type ADC
ii. Good ratio of speed to power
iii. Compact design compared to Flash type ADC

Disadvantages of Successive Approximation ADC

i. Cost is high because of SAR
ii. Complexity in design

R to 2R LADDER NETWORK DIGITAL TO ANALOG CONVERTER (DAC)

Following figure shows the circuit diagram of a 4bit R to 2R weighted resistor DAC.

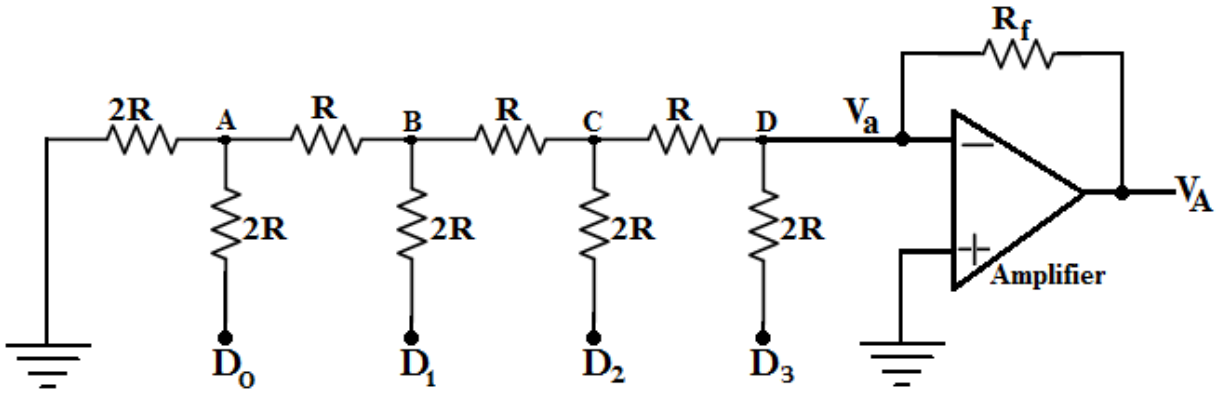

Figure: 4 bit R to 2R weighted ladder network DAC

Working

R to 2R weighted resistor ladder network uses only 2 set of resistors R and 2R as shown in the above figure.

The first two 2R resistors from the left hand side are in parallel (when the digital bit D_0 is LOW (grounded)). Thus, they can be replaced with a single resistor R (as 2R||2R = R). This equivalent resistance R is in series with the resistance R (between A and B). So, they combine to a single resistor of value 2R, which is in parallel with the 2R resistor to D_1. This process repeats itself each time we work from left to right, successively replacing combinations of resistors with their equivalents. The circuit ultimately simplifies to a single resistor R. Thus, the impedance of the R-2R resistor network is always equal to R, regardless of the size (number of bits) in the network.

In the circuit, D_0, D_1, D_2 and D_3 are the input bits (voltage levels). Using Thevenin's theorem, it can be shown that at point A, potential is $D_0/2$ because of the parallel resistors of 2R value. As we proceed towards right hand side,

this voltage reduces to half in every stage (of 2R parallel resistors). Thus, at point B potential due to D_0 is $D_0/4$, at point C $D_0/8$ and finally at point D it is $D_0/16$. Similarly, contribution of D_1 at point D is $D_1/8$, contribution of D_2 is $D_2/4$ and that of D_3 is $D_3/2$. Therefore potential at point D is given by

$$V_a = \frac{D_3}{2} + \frac{D_2}{4} + \frac{D_1}{8} + \frac{D_0}{16}$$

In a more general sense, the contribution of each bit to the output is a simple binary weighting function of each bit. As we move from the MSB to the LSB, the voltage contribution of each bit reduces half. Above equation is an analogous representation of the same.

Say, the two levels of the input voltage are 0V (LOW) and 16V (HIGH).

For an input, D_3=0, D_2=1, D_1=0 and D_0=1, we get $V_a = \frac{0}{2} + \frac{16}{4} + \frac{0}{8} + \frac{16}{16} V$

$= 0 + 4 + 0 + 1 V$ = 5V (we know, 0101_2=5)

Different combinations in the inputs can be verified similarly.

As input voltage may not be of 16V always, the output voltage (V_a) needs to be scaled (amplified or attenuated). Therefore an amplifier is connected at the output of the ladder network.

Advantages

i. Simple, effective, accurate circuit

ii. Easy to develop as resistances with only two values are required

Drawback

i. It has slower conversion rate